## REMARKS

This paper is responsive to the Non-Final Office Action dated July 27, 2005. Claims 1-24 and 26-56 were examined. All claims were rejected.

### *Claim Rejections - 35 U.S.C. § 102*

Claims 1, 2, 8, 9, 13, 14, 18-24, 26-30, 32-33, 37-38, 40-43, 46, 50-53 and 56 stand rejected under 35 U.S.C. § 102(a) as being anticipated by La Rosa (U.S. Patent No. 6,738,286). Applicant traverses this rejection in part, as described below.

Regarding claim 1, the Examiner has advanced the position that La Rosa discloses in Fig. 3, Fig. 4, and Fig. 6 a non-volatile memory cell array comprising within a first array block (COL0) a first plurality of X-lines ($WL_m$ and $WL_{m+1}$) configured to be simultaneously selected in a read mode of operation, and each associated with a first Y-line group (BL0 to BL4) numbering at least one Y-line.

Regarding Fig. 3, the only relevant aspect that is described by La Rosa concerns the two zones B1 and B2, which can be read simultaneously and are erasable independently from one another. The word line decoder WLDEC2 is also arranged to select the word lines $WL_m$ and $WL_{m+1}$ simultaneously during a reading operation (see column 5, lines 25-31). Such a description does not include any insight as to the details of zones B1 and B2, and thus Fig. 3 taken alone poses no issue to any of the claims.

La Rosa provides an example of such zones B1 and B2 in Fig. 4. Applicant respectfully submits that this figure does not show a first plurality of X-lines configured to be simultaneously selected in a read mode of operation, and *each associated with a first Y-line group* numbering at least one Y-line, as recited in claim 1.

Fig. 4 admittedly shows two word lines $WL_m$ and $WL_{m+1}$ which are simultaneously selected in a read mode. However, the word line $WL_m$ is only associated with bit-lines BL5-BL7 and is *not* associated with bit lines BL0-BL4, whereas the other word line $WL_{m+1}$ is only associated with bit-lines BL0-BL4 and is *not* associated with bit lines BL5-BL7. For example, La Rosa recites:

> According to the invention, the drains D of the access transistors AT of the cells C10, C11, C12, C13 and C14 of the zone B1 are not connected to the bit lines $BL_0$, $BL_1$, $BL_2$, $BL_3$, $BL_4$ and the drains D of the access transistors AT of the cells C25, C26, C27 of the zone B1 are not connected to the bit lines $BL_5$, $BL_6$, $BL_7$. The absence of the connections are illustrated in the figure by circled crosses. (column 6, lines 1-7)

A word line cannot be considered as being associated with a bit line unless a memory cell is coupled between such a word line and such a bit line. (See the instant application's consistent usage of "associated", such as on page 2 at lines 7-9, on page 10 at lines 29-30, and elsewhere.) La Rosa includes the "non-useful" memory cells (e.g., C10-C14) to simplify the mask implications of zones B1 and B2, and to ensure that other cells which are coupled to both a word line and a bit line are consistent with the memory cells elsewhere in the array (see column 7 at lines 55-59, and column 8 at lines 6-9). Such non-useful memory cells are *not associated* with the bit line to which it could have been connected, but in fact is not connected.

As another example, La Rosa drives home this structural distinction with the following:

> It follows from the foregoing that an essential and sufficient characteristic for simultaneous reading of the special bits of the first and of the second type is that a line of bits connected to a useful memory cell of a special zone is not connected to a useful memory cell of the other special zone. (column 7, lines 60-64)

With this teaching strongly set forth by La Rosa, it is clear that the word lines $WL_m$ and $WL_{m+1}$ are not *both* associated with the bit lines BL0-BL4, nor are they *both* associated with the bit lines BL5-BL7. Thus Fig. 4 does not show a non-volatile memory cell array comprising within a first array block a first plurality of X-lines configured to be simultaneously selected in a read mode of operation, and *each associated with a first Y-line group* numbering at least one Y-line. Applicant respectfully traverses the rejection as to the alleged teaching of Fig. 4.

In Fig. 6 La Rosa describes another embodiment. The distinctions as between $WL_m$ and $WL_{m+1}$ set forth above are also true in this figure, since the word line $WL_m$ is only associated with the bit line group including BL5-BL7, whereas the word line $WL_{m+1}$ is only associated with the bit line group including BL0-BL4.

However, Fig. 6 also include zones B1' and B2' in addition to zones B1 and B2. The word line $WL_m$' of the zone B1' is connected to the word line $WL_m$ of the zone B1, and the word line $WL_{m+1}$' of the zone B2' is connected to the word line $WL_{m+1}$ of the zone B2. (The specification at column 8, lines 10-13 is clearly in error (e.g., referring to $WL_{m+1}$ being in zone B1) relative to the figure itself.) La Rosa continues with:

> The valid cells of the zones B1' and B2' are in this case read, erased, then programmed at the same time as the corresponding memory cells of the zones B1 and B2. The condition and configuration bits are then subject to a double storing (redundancy), which represents an insurance factor in case of a failing useful memory cell of the zone B1 or of a useful memory cell of the zone B2. (column 8, lines 13-19)

To accomplish this functionality (and as Fig. 6 shows) the word lines $WL_m$ and $WL_m$' are connected together, and so are simultaneously selected during a read mode, during an erase mode, and during a program mode of operation. Likewise, the word lines $WL_{m+1}$ and $WL_{m+1}$' are connected together, and so are simultaneously selected during a read mode, during an erase mode, and during a program mode of operation. La Rosa provides no teaching for any mode of operation not consistent with such a pair of word lines being connected together (and thus either both selected or both unselected for *all* operation modes).

Applicant has amended claim 1 to now recite "... a first plurality of independently selectable X-lines configured to be simultaneously selected in a read mode of operation, and each associated with a first Y-line group numbering at least one Y-line." Applicant respectfully submits that claim 1, as amended, clearly distinguishes over La Rosa, including with regard to Fig. 6, and believes this rejection has been overcome with regard to claim 1.

Regarding independent claims 29 and 51, Applicant respectfully traverses the rejection, and submits that La Rosa nowhere teaches or suggests the recited method or apparatus. Applicant respectfully submits that nowhere does La Rosa describe:

> programming *individual* memory cells associated with a first X-line group of at least one X-line within a first array block and further associated with a first Y-line group of at least one Y-line within the first array block until a desired first *aggregate* memory cell read current is obtained *when simultaneously selecting* all the first group of X-lines and all the first group of Y-lines, at least one of the first X-line group and first Y-line group including more than one such X-line or Y-line; and

reading the memory array by *simultaneously* selecting all the first group of X-lines and all the first group of Y-lines and generating a signal responsive to the first *aggregate* memory cell read current. (e.g., taken from claim 29)

As described above, La Rosa in Fig. 6 shows memory cells that are read, erased, and programmed simultaneously. Nowhere is an aggregate memory cell current described during a read operation.

Regarding independent claim 38, Applicant respectfully traverses the rejection, and submits that La Rosa nowhere teaches or suggests the recited method or apparatus. Applicant respectfully submits that nowhere does La Rosa describe an integrated circuit comprising:

... a Y-line selection circuit for simultaneously selecting within the first array block in the read mode a first Y-line group of at least one Y-line and a second Y-line group of at least one Y-line, and for respectively coupling the selected first and second Y-line groups to respective first and second inputs of an associated sense amplifier circuit;

wherein the associated sense amplifier circuit is responsive to an *aggregate* signal from memory cells associated with *both* the selected *first X-line group* and the selected *first Y-line group*, and responsive to an *aggregate* signal from memory cells associated with *both* the selected *first X-line group* and the selected *second Y-line group*. (e.g., taken from claim 38)

Regarding claim 2, the position advanced in the Office action is traversed in light of the above arguments. In addition, Fig. 3 discloses no such structure.

Regarding claims 19-24, 42, and 43, the position advanced in the Office action is traversed in light of the above arguments. In particular, La Rosa discloses only a single pair of word lines that are simultaneously selected in a read mode of operation. There is no second of third plurality of word lines disclosed that are simultaneously selected in a read mode of operation, let alone that are also each associated with the first Y-line group.

Applicant respectfully submits that this rejection has been overcome, and requests the rejection be withdrawn.

Claims 1-5, 8, 13, 14, 18, 27-30, 32-33, 38, 40, 41, 46, 50-53 and 56 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Zink et al. (U.S. Patent No. 5,946,241). Applicant respectfully traverses this rejection.

Regarding claim 1, the Examiner has advanced the position that La Rosa discloses in Fig. 3 and Fig. 4 a non-volatile memory cell array comprising within a first array block ($COL_0$) a first plurality of X-lines (LMjs) configured to be simultaneously selected in a read mode of operation, and each associated with a first Y-line group ($BL_0$ to $BL_7$) numbering at least one Y-line.

Applicant respectfully submits that Zink clearly teaches otherwise. Zink teaches a memory architecture having two memory cells per stored bit of information. Each of the two memory cells resides in a respective array block (i.e., "half-array"), and the read circuit (i.e., "sense amplifier" circuit) is preferably disposed between the two array blocks. Zink teaches:

> Preferably, the memory array has two parts that are symmetrical with respect to each of said read circuits owing to the fact that the memory cells of one of these parts are connectable exclusively to one of said first and second terminals of said read circuits while the memory cells of the other part are connectable exclusively to the other of said first and second terminals of said read circuits.
>
> Thus, for each bit, the programmed cell will belong to one part of the memory array while the erased cell will belong to the part that is symmetrical to it. (column 4, lines 1-10)

Zink clearly sets forth two array blocks, separated by a group of read circuits. The selected word line LMj in the upper portion of Fig. 3, and the selected word line LMj in the lower portion of Fig. 3, are thus respectively disposed within *different* array blocks. Zink continues:

> According to the invention, the memory array has programmed and an erased memory cell *on either side of a plurality of read circuits* $CL'_0, \ldots, CL'_7$. Consequently during the reading stage, for each bit of a word only the erased cell consumes current. A read circuit is described here below in FIG. 4.
>
> In order to obtain a perfectly symmetrical memory array, the memory array is *divided into two identical half-arrays*: an upper half-array and a lower half-array. Each half-array is identical to the part of the memory array pertaining to cell $C_i$ described in FIG. 1. Each read circuit $CL'_0, \ldots, CL'_7$ is associated firstly with a plurality of bit lines $LB'_0, LB'_i, LB'_{i+7}, \ldots$ belonging to the upper half-array and secondly to a plurality of bit lines $LB'_0, LB'_i, LB'_{i+7}, \ldots$ belonging to the lower half-array. Memory cells $C_i$

> and $C'_i$ are respectively connected to bit lines $LB_i$ and $LB'_i$. The read circuits are preferably located between the two half-arrays. The perfect symmetry of the memory array provides for a simultaneous selection of the memory cells $C_i$ and $C'_i$ in both half-arrays. (column 4, line 51 through column 6, line 3)

Zink discloses a memory structure in which more than one word line may be simultaneously activated, but such word lines are located within different half-arrays (i.e., "memory blocks"). In addition, the bit lines within one half-array are distinct from the bit lines within the other half array. Alternatively, if such two word lines are connected together to form a single electrical node, and if such a compound word line is thought of as a single word line, then there is only *one* word line is selected at a time.

In Fig. 4, Zink describes a read circuit useful for his invention. In this figure he shows a single word line LMj coupling a memory cell $C_i$ to the bit line $LB_i$ and also coupling a memory cell $C'_i$ to the bit line $LB'_i$. Since this figure is introduced to describe the read circuit, the word line structure might be assumed to be a non-physical representation of the equivalent circuit shown in Fig. 3 with regard to a selected word line in each of the two half-arrays. However, if this figure is taken to teach a different physical structure than taught by Fig. 3, then the two memory cells $C_i$ and $C'_i$ *could* possibly be thought of as being disposed within a single array block. But if that is the case, then there is only a *single* word line LMj selected at one time during a read operation. It is unlikely that Zink means to suggest this possibility, as the text clearly describes Fig. 4 in the context of Fig. 3:

> FIG. 4 shows a read circuit $CL'_k$ of the non-volatile memory according to the invention. This read circuit is connected firstly to bit line $LB_i$ and secondly to bit line $LB'_i$. *According to FIG. 3*, memory cells $C_i$ and $C'_i$ are connected respectively to bit lines $LB_i$ and $LB'_i$ and are selected by word line $LM_j$. Upon receipt of signal $COL_p$, the $p_{th}$ word is read, by coupling eight respective bit lines $LB_i$ through $LB_{1+7}$ [sic] and $LB'_i$ through $LB'_{1+7}$ [sic] to their respective reading circuits $CL'_0$ through $CL'_7$.
> (column 5, lines 41-49) [the subscripts "1+7" clearly should be "i+7"]

However, under either assumption, it is still clear that Zink does not teach or suggest a non-volatile memory cell array comprising within a first array block a first plurality of X-lines configured to be simultaneously selected in a read mode of operation, and each associated with a

first Y-line group numbering at least one Y-line. Even the unamended claim 1is thus shown to distinguish over Zink.

Regarding independent claims 29, 38, and 51, Applicant respectfully traverses the rejection, and submits that Zink nowhere teaches or suggests the recited method or apparatus for the same reasons as set forth above regarding La Rosa.

*Claim Rejections - 35 U.S.C. § 103*

Claims 10-12, 14-17, 26, 31, 34-36, 44, 45, 47-49, 54, and 55 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over La Rosa (U.S. Patent No. 6,738,286) or Zink et al. (U.S. Patent No. 5,946,241). Applicant respectfully submits that such dependent claims are allowable at least for their dependence from an allowable independent claim, and requests this rejection be withdrawn.

Regarding claims 10-12, 26, 31, 34-36, 44, 45, 54, and 55, the Examiner advances the position that "[i]t would have been obvious to one having ordinary skill in the art at the time the invention was made to modify La Rosa and Zink' non-volatile EEPROM with the different types of non-volatile memories as the claimed invention since they have the same purpose and advantages to retain recorded information even when the power to the memory is turned off and *since it has been held that constructing a formerly memory structure [sic] in various elements involves only routine skill in the art* (see Zink col. 6, lines 24-32)."

The cited portion of Zink recites:

> Having thus described at least one illustrative embodiment of the invention, various alterations, modifications, and improvements will readily occur to those skilled in the art. Such alterations, modifications, and improvements are intended to be within the spirit and scope of the invention. Accordingly, the foregoing description is by way of example only and is not intended as limiting. The invention is limited only as defined in the following claims and the equivalents thereto.
> (column 6, lines 24-32)

This cited portion can hardly be viewed as providing the suggestion alleged by the Examiner.

Regarding claims 14-17 and 47-49, the Examiner advances the position that "[i]t would have been obvious to one having ordinary skill in the art at the time the invention was made to modify La Rosa and Zink' memory array with the different dimensional memory array [sic] and disposal [sic] one or more layers of the memory array as the claimed invention, *since it has been held that constructing a formerly memory array in various dimensions and layers involves only routine skill in the art* (see Zink col. 6, lines 24-32)."

Again , this cited portion can hardly be viewed as providing the suggestion alleged by the Examiner. As a specific example regarding claims 16 and 48, it is emphatically believed that there is no suggestion in the cited art, nor in general knowledge of one having ordinary skill in the art, for the first plurality of X-lines (or the first group of X-lines) comprising X-lines disposed on more than one layer of the memory array, as recited in the claims.

Claims 6, 7 and 39 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over La Rosa (U.S. Patent No. 6,738,286) or Zink et al. (U.S. Patent No. 5,946,241) in view of Yero (U.S. Patent No. 5,986,937).

The Examiner advances the position that "it would have been obvious to a person of ordinary skill in the art at the time the invention was made to add the reference signal or the current source to La Rosa and Zink's sense amplifier as taught by Yero *in order to reduce the borderline value of the precharging potential of the bit lines* (col. 1, lines 5-10 and col. 2, lines 61-64)." Applicant respectfully submits that such motivation stated by Yero bears no relationship to the claimed invention. Moreover, Applicant respectfully submits that such dependent claims are allowable at least for their dependence from an allowable independent claim, and requests this rejection be withdrawn.

The various dependent claims, even if not individually argued herein, are believed allowable at least for their dependence from an allowable independent claim. Applicant's silence as to any rejection of such dependent claim is not to be taken as acquiescence to the basis of such rejection.

*Summary*

Claims 1-24 and 26-56 remain in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited.

Should any issues remain, Applicant respectfully requests a telephonic interview with the Examiner to discuss this response, and further in the hope that the remaining issues might be efficiently resolved.

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Andrew C. Graham 10-27-05 Date

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